Electronic Version
Stylesheet Version v1.1.1

WAFER ACCEPTANCE TESTING METHOD AND STRUCTURE OF A TEST KEY USED IN THE METHOD

Abstract

A wafer acceptance testing (WAT) method for monitoring GC-DT misalignment and a test key structure are disclosed. The test key includes a deep trench capacitor structure biased to a first voltage (V_{DT}). The deep trench capacitor structure is formed in a substrate, on which active areas are defined. The deep trench capacitor structure includes a buried strap out diffusion region that is formed within the active area and is electrically connected to the deep trench capacitor structure. The deep trench capacitor structure is isolated by shallow trench isolation (STI). A GC-T electrode layout and a GC-B electrode layout are formed over the substrate. The GC-T electrode layout, which is biased to a second voltage (V_{GC-T}), includes a plurality of columns of GC-T fingers. The GC-B electrode layout, which is biased to a third voltage (V_{GC-B}), includes a plurality of columns of GC-B fingers that interdigitate the plurality of columns of GC-T fingers over the active areas and STI. A first capacitance C_1 of a first capacitor contributed by the plu-

rality of columns of GC-T fingers and the buried strap out diffusion region is measured. A second capacitance C_2 of a second capacitor contributed by the plurality of columns of GC-B fingers and the buried strap out diffusion region is measured. The first capacitance C_1 and second capacitance C_2 are compared, wherein when $C_1 \neq C_2$, GC-DT is misaligned.